



# LOW VOLTAGE CMOS 16-BIT D-TYPE FLIP-FLOP (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
  - $f_{MAX} = 150MHz$  (MIN.) at  $V_{CC} = 3V$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE: |I<sub>OH</sub>| = I<sub>OI</sub> = 24mA (MIN) at V<sub>CC</sub> = 3V
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS: t<sub>PLH</sub> ≅ t<sub>PHL</sub>
- OPERATING VOLTAGE RANGE:
   V<sub>CC</sub>(OPR) = 2.0V to 3.6V (1.5V Data
- Retention)

  PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16374
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE: HBM > 2000V (MIL STD 883 method 3015); MM > 200V

#### **DESCRIPTION**

The 74LCX16374 is a low voltage CMOS 16 BIT D-TYPE FLIP-FLOP with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs.

These 16 bit D-TYPE flip-flops are controlled by two clock inputs (nCK) and two output enable inputs(nOE). On the positive transition of the (nCK), the nQ outputs will be set to the logic state that were setup at the nD inputs. While the (nOE) input is low, the 8 outputs (nQ) will be in a normal state (high or low logic level) and while high level the outputs will be in a high impedance state.

Any output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

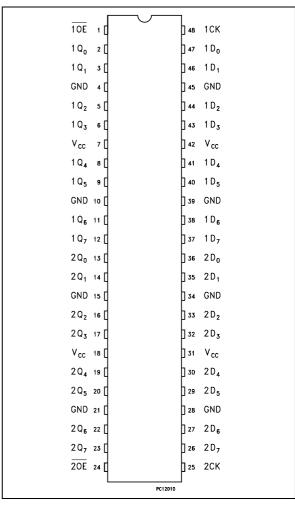
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



#### **ORDER CODES**

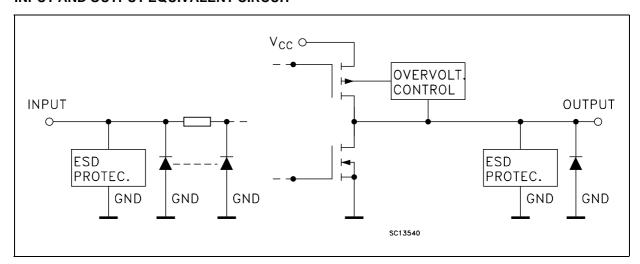
PACKAGE	TUBE	T&R
TSSOP		74LCX16374TTR

#### **PIN CONNECTION**



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#### INPUT AND OUTPUT EQUIVALENT CIRCUIT



#### **PIN DESCRIPTION**

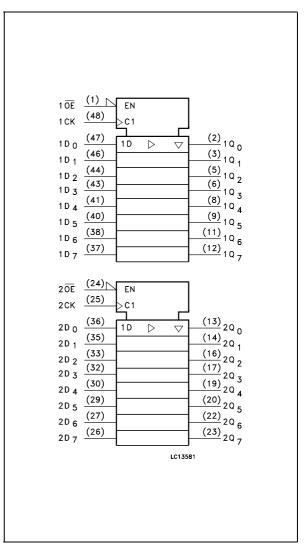
PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2CK	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1CK	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive Supply Voltage

#### **TRUTH TABLE**

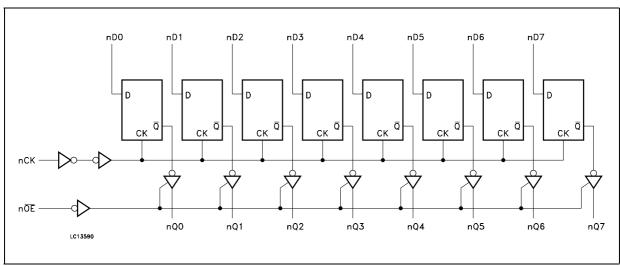
	OUTPUT		
OE	СК	D	Q
Н	Х	Х	Z
L		Х	NO CHANGE*
L		L	L
L	J	Н	Н

X : Don't Care Z : High Impedance

#### **IEC LOGIC SYMBOLS**



#### **LOGIC DIAGRAM**



This logic diagram has not to be used to estimate propagation delays

#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
Vo	DC Output Voltage (OFF State)	-0.5 to +7.0	V
Vo	DC Output Voltage (High or Low State) (note 1)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	- 50	mA
I <sub>OK</sub>	DC Output Diode Current (note 2)	- 50	mA
Io	DC Output Current	± 50	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	± 100	mA
$I_{GND}$	DC Ground Current per Supply Pin	± 100	mA
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

1) I<sub>O</sub> absolute maximum rating must be observed

2) V<sub>O</sub> < GND

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage (note 1)	2.0 to 3.6	V
V <sub>I</sub>	Input Voltage	0 to 5.5	V
Vo	Output Voltage (OFF State)	0 to 5.5	V
Vo	Output Voltage (High or Low State)	0 to V <sub>CC</sub>	V
I <sub>OH</sub> , I <sub>OL</sub>	High or Low Level Output Current (V <sub>CC</sub> = 3.0 to 3.6V)	± 24	mA
I <sub>OH</sub> , I <sub>OL</sub>	High or Low Level Output Current (V <sub>CC</sub> = 2.7V)	± 12	mA
T <sub>op</sub>	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

<sup>1)</sup> Truth Table guaranteed: 1.5V to 3.6V 2) V<sub>IN</sub> from 0.8V to 2V at V<sub>CC</sub> = 3.0V



#### **DC SPECIFICATIONS**

		Te	est Condition					
Symbol Parameter	Parameter	v <sub>cc</sub>		-40 to	85 °C	-55 to	125 °C	Unit
		(V)		Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
$V_{IL}$	Low Level Input Voltage	2.7 10 3.6			0.8		0.8	V
V <sub>OH</sub>	High Level Output	2.7 to 3.6	I <sub>O</sub> =-100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		
	Voltage	2.7	I <sub>O</sub> =-12 mA	2.2		2.2		V
		2.0	I <sub>O</sub> =-18 mA	2.4		2.4		V
		3.0	I <sub>O</sub> =-24 mA	2.2		2.2		
V <sub>OL</sub>	Low Level Output	2.7 to 3.6	I <sub>O</sub> =100 μA		0.2		0.2	
	Voltage	2.7	I <sub>O</sub> =12 mA		0.4		0.4	V
		3.0	I <sub>O</sub> =16 mA		0.4		0.4	V
		3.0	I <sub>O</sub> =24 mA		0.55		0.55	
I <sub>I</sub>	Input Leakage Current	2.7 to 3.6	V <sub>I</sub> = 0 to 5.5V		± 5		± 5	μА
I <sub>off</sub>	Power Off Leakage Current	0	$V_{I}$ or $V_{O} = 5.5V$		10		10	μА
I <sub>OZ</sub>	High Impedance Output Leakage Current	2.7 to 3.6	$V_I = V_{IH} \text{ or } V_{IL}$ $V_O = 0 \text{ to } V_{CC}$		± 5		± 5	μА
I <sub>CC</sub>	Quiescent Supply	2.7 to 2.6	$V_I = V_{CC}$ or GND		20		20	^
Current	Current	2.7 to 3.6	$V_{I}$ or $V_{O}$ = 3.6 to 5.5 $V$		± 20		± 20	μΑ
$\Delta I_{CC}$	I <sub>CC</sub> incr. per Input	2.7 to 3.6	$V_{IH} = V_{CC} - 0.6V$		500		500	μΑ

#### **DYNAMIC SWITCHING CHARACTERISTICS**

		Tes	Value				
Symbol Parameter		v <sub>cc</sub>		٦	Γ <sub>A</sub> = 25 °C	;	Unit
		(V)		Min.	Тур.	Max.	,
V <sub>OLP</sub>	Dynamic Low Level Quiet	3.3	$C_L = 50pF$ $V_{IL} = 0V, V_{IH} = 3.3V$		0.8		V
V <sub>OLV</sub>	Output (note 1)	3.3	$V_{IL} = 0V, V_{IH} = 3.3V$		-0.8		V

<sup>1)</sup> Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

#### **AC ELECTRICAL CHARACTERISTICS**

		Test Condition				Value					
Symbol	Parameter	V <sub>CC</sub>	CL	R <sub>L</sub>	t <sub>s</sub> = t <sub>r</sub>	-40 to 85 °C		-55 to	125 °C	Unit	
		(V)	(pF)	(Ω)	(ns)	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay	2.7	50	500	2.5	1.5	6.5	1.5	6.5	ns	
	Time	3.0 to 3.6	50	500	2.5	1.5	6.2	1.5	6.2	115	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	2.7				1.5	6.3	1.5	6.3		
	to HIGH and LOW level	3.0 to 3.6	50	50 500	2.5	1.5	6.1	1.5	6.1	ns	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	2.7				1.5	6.2	1.5	6.2		
	from HIGH and LOW level	2 0 to 2 6	3.6	50 500	2.5	1.5	6.0	1.5	6.0	ns	
t <sub>S</sub>	Set-Up Time, HIGH	2.7					2.5		2.5		
	or LOW level (Dn to CK)	3.0 to 3.6	50	500	2.5	2.5		2.5		ns	
t <sub>h</sub>	Hold Time, HIGH or	2.7				1.5		1.5			
	LOW level (Dn to CK)	3.0 to 3.6	50	500	2.5	1.5		1.5		ns	
$t_{W}$	CK Pulse Width,	2.7	50	500	2.5	3.0		3.0		ns	
	HIGH or LOW	3.0 to 3.6	30	300	2.5	3.0		3.0		115	
$f_{MAX}$	Clock Pulse Frequency	3.0 to 3.6	50	500	2.5	170		150		MHz	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns	

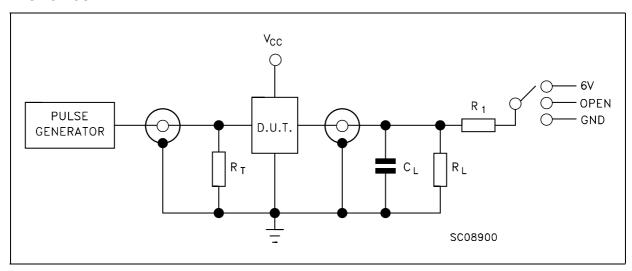
<sup>1)</sup> Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (toshh = | tolhh - tolhh -

#### **CAPACITIVE CHARACTERISTICS**

		Tes	Value				
Symbol	Symbol Parameter			7	Γ <sub>A</sub> = 25 °C	;	Unit
		(V)		Min.	Тур.	Max.	
C <sub>IN</sub>	Input Capacitance	3.3	$V_{IN} = 0$ to $V_{CC}$		7		pF
C <sub>OUT</sub>	Output Capacitance	3.3	$V_{IN} = 0$ to $V_{CC}$		8		pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3	$f_{IN} = 10MHz$ $V_{IN} = 0 \text{ or } V_{CC}$		20		pF

<sup>1)</sup> C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $C_{C(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$  (per circuit)

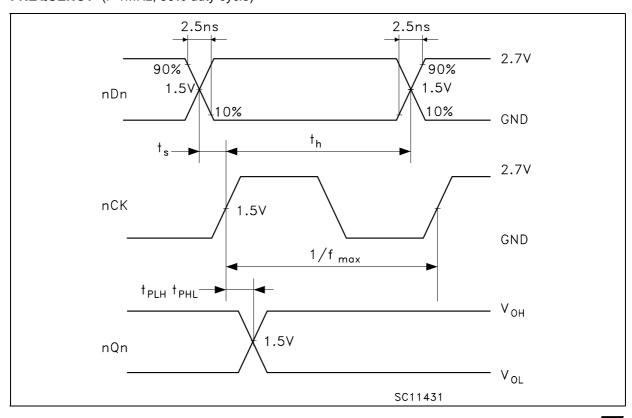
#### **TEST CIRCUIT**



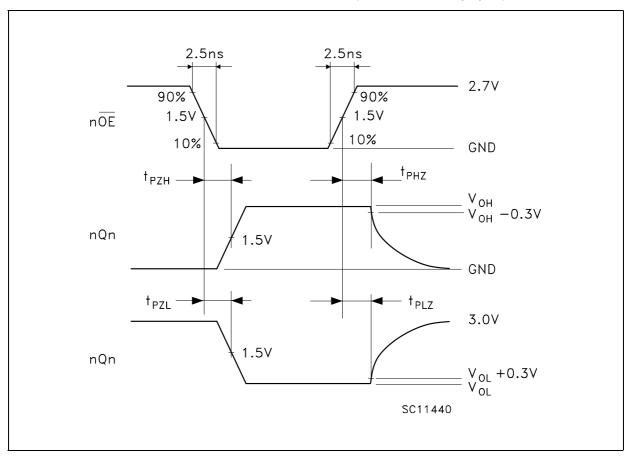
TEST	SWITCH
t <sub>PLH</sub> , t <sub>PHL</sub>	Open
t <sub>PZL</sub> , t <sub>PLZ</sub>	6V
t <sub>PZH</sub> , t <sub>PHZ</sub>	GND

 $C_L$  = 50 pF or equivalent (includes jig and probe capacitance)  $R_L$  = R1 = 500 $\Omega$  or equivalent  $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50 $\Omega$ )

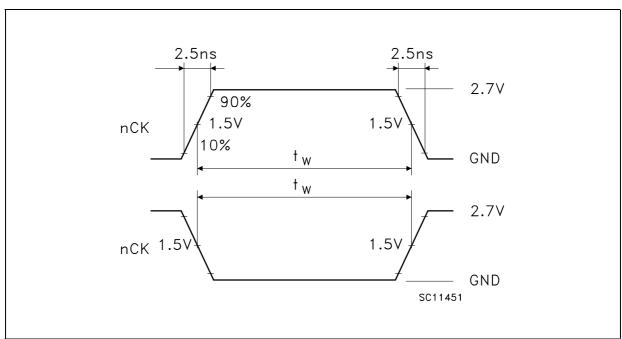
### WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES, MAXIMUM CLOCK FREQUENCY (f=1MHz; 50% duty cycle)



#### WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

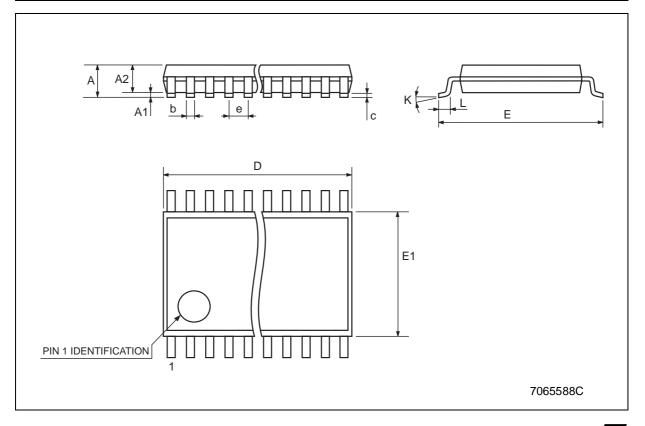


## WAVEFORM 3: PULSE WIDTH (f=1MHz; 50% duty cycle)



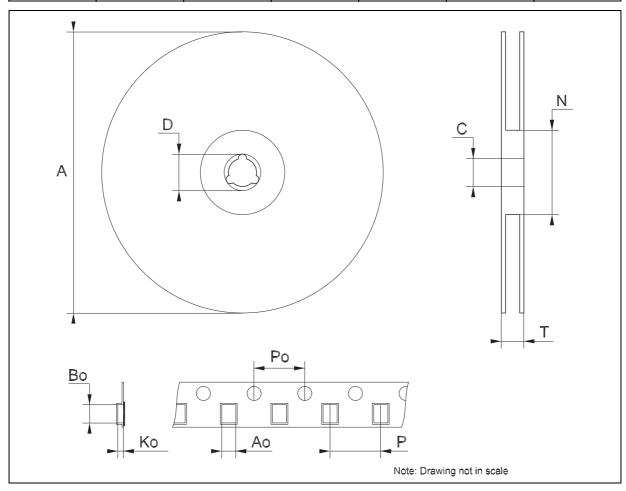
# **TSSOP48 MECHANICAL DATA**

DIM.		mm.			inch	
DIWI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
С	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
е		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



# Tape & Reel TSSOP48 MECHANICAL DATA

DIM		mm.				
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			330			12.992
С	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
Т			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Во	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
Р	11.9		12.1	0.468		0.476



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